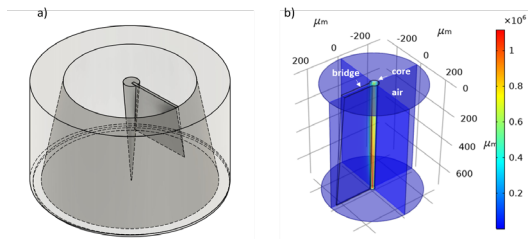


Integrated Optical Waveguide

INVENTION

A silicon waveguide etched through the full thickness of a silicon chip has the potential to greatly reduce the superficial space occupied by coupling structures and simultaneously pave the way for 3D advanced photonic chip packaging solutions. The integrated optical waveguide is realized by deep reactive ion etching, which is a well-established process in the CMOS industry. Therefore, this component can be directly implemented in the large-scale production of 200- or 300-mm large wafers. This manufacturing method additionally allows to obtain sloped sidewalls, which can provide the necessary transition from micrometric optical fibers to nanometric silicon waveguides over a length of hundreds of micrometers. In this way, an adiabatically tapered link to the optical network can be generated without sacrificing space on the chip's surface.

FIGURES:



- a) Design of a tapered optical integrated waveguide with a suspended bridging structure.
b) 3D beam propagation simulation of a bridged optical through-silicon waveguide with a tapering angle of 0.9° .

In fact, the size of the two end faces of the integrated waveguide should be matched with the size of the light source and of the coupling element whose dimension can be vastly reduced in comparison to direct coupling. Moreover, similarly to the through-silicon vias (TSVs) technology, connections in the vertical direction are enabled. This unlocks the opportunity of stacking electro-optical chips on the top of each other to reach unbelievably highly efficient optical networks in a tight and compact package. The integrated optical waveguide is surrounded by an annular hole which is partially interrupted by a bridging structure necessary to assure the required mechanical stability. The waveguide cladding can be realized using different materials such as SiO_2 , Si_3N_4 or simply air.

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INTELLECTUAL PROPERTY

- European patent application EP4083671 A1, filing date 27.04.2021, PCT patent application WO2022/228790 A1, filing date 24.03.2022, co-owned with IHP GmbH, pending
- Stage of technological development: proof of principle
- IP-commercialization: open for R&D collaboration, licensing or patent sale